AMENDMENTS TO THE CLAIMS

1. through 57. (Cancelled)

58. (Original) A method of forming integrated circuitry comprising:

providing a transistor array over a substrate;

providing a digit line over said transistor array;

providing a plurality of layers of material over said digit line;

forming one of square, rectangular, and oval pattern in at least one of said plurality of layers of material, said pattern being defined by having raised structures alternating with recesses;

transferring said pattern into an underlying layer in said plurality of layers;

forming sidewall spacers on vertical surfaces of said transferred pattern; and

forming a capacitor container array defined by said sidewall spacers.

59. (Original) The method according to claim 58 further comprising forming capacitors in said containers.

60. (Original) The method according to claim 58 further comprising forming cell node polysilicon plugs extending above said digit line.

61. (Original) The method according to claim 58 further comprising etching only the top layer of said plurality of layers of material to from said pattern.

62. (Original) The method according to claim 58 further comprising etching two or more of said plurality of layers of material to form said pattern.

63. (Original) The method according to claim 58 further comprising forming a metal layer on top of said pattern.

64. (Original) The method according to claim 63 wherein said metal layer consists of one of titanium, palladium, and tungsten.

65. (Original) The method according to claim 63 further comprising annealing said metal layer to form a silicide.

66. (Original) The method according to claim 58 wherein said plurality of layers of material comprises a BPSG layer between a polysilicon layer and a nitride layer.

67. (Original) The method according to claim 58 wherein said plurality of layers of material comprises a nitride layer beneath a BPSG layer, a polysilicon layer over said BPSG layer, and a TEOS layer over said polysilicon layer.

68. (Original) The method according to claim 58 wherein said plurality of layers of material comprises a nitride layer beneath one of a PSG and a BPSG layer, a polysilicon layer over said one of BPSG and PSG layer, and a TEOS layer over said polysilicon layer.

69. (Original) The method according to claim 58 wherein said sidewall spacers comprise polysilicon spacers.

70. (Original) The method according to claim 58 wherein said sidewall spacers comprise titanium nitride spacers.

71. (Original) The method according to claim 58 wherein said sidewall spacers comprise TEOS spacers that are etched from between the capacitors.

72. (Original) The method according to claim 58 wherein said sidewall spacers comprise platinum spacers.

73. (Original) The method according to claim 58 wherein said sidewall spacers comprise amorphous silicon spacers.

74. (Original) The method according to claim 73 further comprising seeding and annealing said spacers to form an HSG layer.

75. (Original) The method according to claim 58 wherein said capacitors are formed as metal insulator metal capacitors.

76. (Original) The method according to claim 75 wherein said capacitors comprise a first platinum layer, a Ta_2O_5 or BST layer, and a second platinum layer.

77. (Original) The method according to claim 76 further comprising forming a conductive barrier layer beneath either the first or second platinum layer.

78. (Original) The method according to claim 77 wherein said conductive barrier layer comprises tantalum nitride or tantalum silicon nitride.

79. (Original) The method according to claim 58 wherein said capacitors are formed as metal insulator silicon capacitors.

80. (Original) The method according to claim 79 wherein said capacitors comprise an HSG layer, a Ta_2O_5 layer, and a titanium nitride layer.

81. (Original) The method according to claim 58 wherein said spacers are electrically connected to a cell plate and function as part of the cell plate of the capacitor.

82. through 113. (Cancelled)

114. (Original) The method according to claim 58 wherein said sidewall spacers comprise TEOS spacers and are left between said capacitors.

115. and 116. (Cancelled)